REMARKS

Claim Rejections 35 USC 112

The rejection of claims 1 – 5, 7 – 10, 15 and 16 under 35 USC 112 is respectfully traversed.

See the accompanying Declaration by one of the inventors.

The examiner has objected that "the disclosure lacks an adequate description regarding what is in the recited chemical constituent, how it is introduced - - and how such steps could be controllable".

Applicants maintain that these steps are conventional in the field of integrated circuit formation and that therefore they are known to those skilled in the art.

For example, the chemical constituents are the same as those used in planar FET technology; they are introduced by opening a valve to add a precursor

to the gas flow in a CVD, PEVCD, sputter, etc. tool at a time when the bottom or top of the nanotube is being formed; and they are controlled by adjusting the valve to vary the flow rate at the time when the bottom or top of the nanotube is being formed.

As an example of a technique known in the art, the reference cited by Roesner on the bottom of column 1 establishes that techniques for doping carbon nanotubes with boron or nitrogen, two well known dopant materials, are known in the art.

In the response of 06/27/2005, the Examiner has stated "the example of Roesner about doping carbon nanotube with boron and nitrogen: - - is not particularly relevant to the raised concerns, since these dopants in Roesner are intended to be used to form an insulating nanotube - ". This statement by the examiner is understood to contain an implied assertion that adding a precursor gas to a CVD chamber is not understood by those skilled in the art.

Applicants firmly maintain that the process of adding additional precursor gases to a CVD process is well understood in the art and note that the Examiner has made no attempt to establish a prima facie case to the contrary.

Applicants remind the examiner that he is required to establish a prima facie case that one skilled in the art would NOT know how to perform these stock, conventional steps in integrated circuit processing. If the Examiner persists in this '112 rejection, Applicants demand that he produce a reference stating that it is not known how to add an additional precursor gas to a CVD process of forming a carbon nanotube.

Claim Rejections 35 USC 103

The rejection of claims 1 - 5, 7 - 10, 15 and 16 under 35 USC 103(a) is respectfully traversed.

Claim 1, as amended, incorporates the limitations of claim 6 and requires that only one of the top and bottom of the nanotube is selectively doped. This permits the remainder of the nanotube to have properties not affected by the doping, in contrast to the prior art which was forced to dope both the source and drain (and channel regions near source and drain) the same or to construct expensive masks to block an implant.

Support is provided in paragraph 49.

The thickness limitation, supported by paragraph 47, specifies more clearly the great uniformity in channel length provided by the present invention. In contrast, Roesner contains no teaching of the much improved channel length uniformity provided by the invention.

In particular, the Examiner's assertion on page 4, lines 3 - 4, that the gate layer "naturally has a thickness that is naturally within a certain thickness tolerance" is incorrect. The gate layer in Roesner will have a thickness range that can be expressed by x%, three sigma, but the value of x will not inherently fall within the tolerance set by the circuit designer. The Examiner is reminded that a thickness tolerance is a cap on the variation of

thickness that is set in order to have the circuit function as specified. The deposition of a layer will certainly not inherently fall within that cap.

The limitation of forming the carbon nanotube after the insulating layer within the aperture (supported by paragraphs 39, 40 and 41 and Figs 6 and 7) is provided to distinguish over the Roesner reference, which shows in Figs 1B and 1C and in Col. 6, lines 24 - 31 the opposite sequence.

The gap between the nanotube and the gate must be small in order to have a functioning gate in contemporary practice of small gate voltages. Use of a process to form the gate electrode after the nanotube, whether by oxidation or deposition, would produce a gate electrode of uneven thickness that would not function properly

Fitch shows a process for forming a silicon FET using conventional deposition processes.

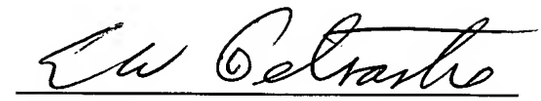
The Examiner has stated that "it would have been obvious to one of ordinary skill - - to make vertical FETs using the method of Roesner, per the teachings of Fitch"

This undercuts the Examiner's arguments with respect to the '112 rejection. The two references can only be combined if the teachings about adding dopants, controlling the process, etc. are known in the art. Thus, the Examiner's assertions in discussing the '112 rejection are proved invalid by his own example.

If the Examiner persists in the '112 rejection, he must drop the suggested combination of Roesner and Fitch, thus undermining the rejection under 35 USC 103.

For the foregoing reasons, allowance of the claims is respectfully solicited.

Respectfully submitted,



by: Eric W. Petraske, Attorney
Registration No. 28,459
Tel. (203) 798-1857